

NARROW BAND QUASI-CIRCULATOR MODULE DESIGN USED IN A TRANSMIT / RECEIVE MODULE

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Abstract

This paper presents the design and the measured performances of a narrow band MMIC quasi-circulator module. Its design implements active divider and combiner. The device demonstrates a noise figure of 5.5 dB and an output power of 18 dBm with associated gains of 4 dB and 7.6 dB for the receive and transmit path, respectively.

Introduction

A quasi-circulator is a three-port network that allows to transmit power from port (1) to port (2) and from port (2) to port (3) [1,2,3]. At present, there are no published results concerning an active device allowing to transport simultaneously a high power signal from transmitter to antenna and a weak power signal from antenna to receiver. This problem has been studied by P.Katzin [2], but his paper describes successively the performances of two different circulators. One presents a noise figure greater than 8.5 dB and an insertion loss of 2 dB, the other allows to obtain an output power of 1 W but with a 12 dB noise figure in the receive-path.

In this paper, we propose a circuit allowing to optimize simultaneously the noise figure and the available output power of an active quasi-circulator. The analyzed frequency band is 3.8-4.2 GHz.

Quasi-circulator module

Fig. 1 shows the block diagram of the quasi-circulator module (QCM). The device is realized by connecting the output ports of the in-phase divider to the input ports of the out-of-phase combiner. The operating principle of this QCM is as follows :

A signal from port (1) gives two in-phase signals to the out-of-phase combiner. A shunt impedance Z_c equal to the reference impedance of port (2) of the QCM is connected to the other port of the in-phase divider in order to have the same magnitude of the signals to the out-of-phase combiner. These two signals will be completely canceled by the combiner. Therefore, the incident signal does not appear at port (3) ($S_{31}=0$). One part of the divider output signal is available at port (2) of the QCM. The divider is an active element so that we can obtain a gain G_1 from port 1 to port 2, thus $S_{21}=G_1$. $S_{12}=0$ because the divider is unilateral.

On the other hand, by connecting a generator at port (2) and thanks to both 90° phase shifters, two out-of-phase signals will be available at the input ports of the combiner. These signals are added by the active combiner, then $S_{32}=G_2$ (gain of the second stage). The combiner is unilateral, thus $S_{23}=0$. In the same way, we can conclude that $S_{13}=0$ because the two ports are linked by two non reciprocal devices (divider and combiner).

The divider is achieved by using a common source

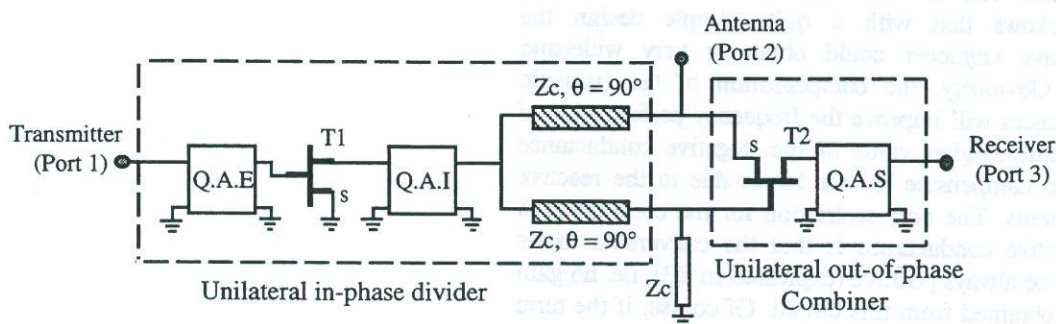


Figure 1: Block diagram of the quasi-circulator module.

transistor T1, a matching two-port (Q.A.E) at port (1), an interstage matching two-port (Q.A.I) and a junction made of two 90° phase shifters. The combiner consists of a transistor T2 and a matching two-port (Q.A.S) network at port (3).

The noise figure calculation

Before optimizing the noise figure F_{23} between ports (2) and (3), it is necessary to know its minimum value if the transistor T2 is a noiseless three-port. For this purpose, we have used a simple model in which the transistor T2 is represented by its transconductance g_m . Similarly, the noise behavior of the circuit constituted of the impedance Z_c (the 50 Ω load at port (1)), the transistor T1 and the two-port Q.A.I has been modeled by an output equivalent impedance Z_1 and a noise current source i_1 (fig. 2). Moreover, the circuit (fig. 2) is constituted of two other impedances :

- The load impedance Z_c at port (2) which is at the standard temperature T_0 (290°K).
- The shunt impedance Z_c between the divider and combiner which is at the room temperature T_a (300°K).

These three impedances generate three noise current sources i_1 , i_{c1} , and i_{c2} , respectively. It is straightforward to calculate the noise current i_s at the output impedance Z' :

$$i_s = \frac{g_m Z_c}{1 + g_m Z_c} (i_{c1} - i_{c2}) \quad (1)$$

This result shows that the noise generated by the transistor T1 has no influence on the receive-path, because i_s is independent of the noise source i_1 and is independent of the impedance Z_1 . This result is due to the perfect symmetry of the circuit in comparison with the axis passing by port (1) and port (3) of the QCM. By definition of a two-port noise figure [4], the noise figure F_{23} of the quasi-circulator will be simply expressed as :

$$F_{23} = \frac{T_0 + T_a}{T_0} \quad (2)$$

This equation shows that the QCM noise figure will be greater than 3.1 dB even if the QCM is realized with a noiseless transistor T2. Owing to the symmetry of the circuit, there is an equal influence of the impedance Z_c of port (2) and of the shunt impedance Z_c . Therefore, one cannot change the shunt impedance Z_c to improve the noise figure F_{23} . The alone foreseeable solution consists to cool the circuit of the QCM. This leads to decrease the room temperature T_a of the shunt impedance Z_c . Consequently, the noise figure F_{23} of the QCM will be improved. In the actual case, T2 is a transistor of F20 technology of GMMT foundry with $0.5 \times 350 \mu\text{m}^2$ gate dimensions and biased at $I_{ds} = I_{dss}/5$, where I_{dss} is the saturated drain current. The calculation of the noise figure F_{23} has been done with the software LIBRA [5]. We have closed port (1) of the QCM by a load impedance $Z_c = 50 \Omega$. This has led us to calculate the noise figure F_{23} of a two-port network instead of the three-port network. In this case, the two MESFETs T1 and T2 are characterized by their specific noise parameters and that the whole resistances of the circuit have been carried at the room temperature T_a (300°K). At the frequency of 4 GHz, the simulated noise figure F_{23} of the QCM is equal to 5.3 dB.

The power optimisation

The transistor T1 is a common source MESFET, with a gate area of $0.5 \times 700 \mu\text{m}^2$ and biased for class AB operation. By using the Curtice nonlinear model, we have obtained the optimum load impedance value of T1 that gives the maximum output power. Then, the elements of the two-port network Q.A.I (fig. 1) have been calculated so that the transistor T1 is terminated by its optimum load impedance. In this case, the output power at port (2) of the QCM is 20 dBm at 1 dB compression point.

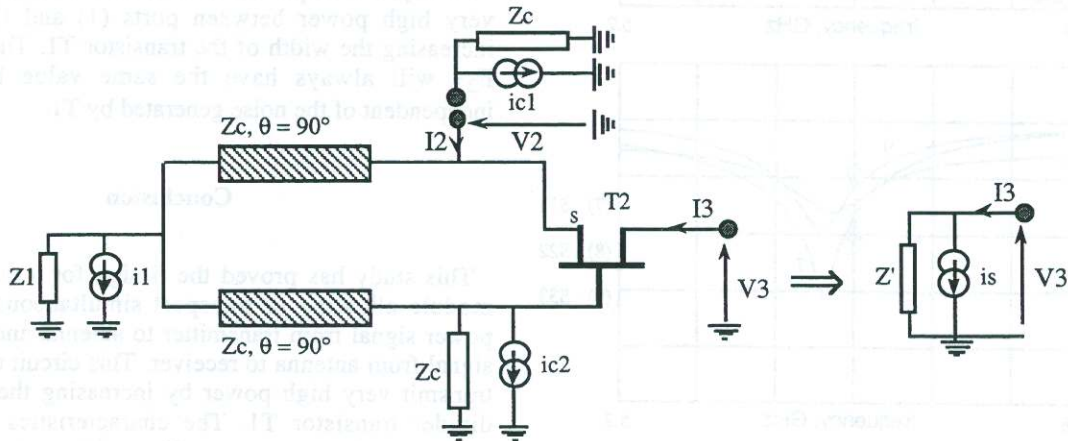


Figure 2: Simplified circuit configuration to calculate the noise figure F_{23} .

Measurement results and comments

The layout drawing of the QCM is shown in fig. 3. Its overall size is about 5 mm^2 . The input matching network Q.A.E is realized by two inductances L1 and L2. The values of these two elements ($L1=3 \text{ nH}$ and $L2=3.5 \text{ nH}$) have been calculated to transform the gate impedance of the transistor T1 to the 50Ω impedance. Similarly, the inductance $L3=5.5 \text{ nH}$ and the capacitor $C3=0.14 \text{ pF}$ constituting the output matching network Q.A.S are determined to match the output of the transistor T2. Port (2) of the QCM is matched thanks to the low input impedance presented by the source

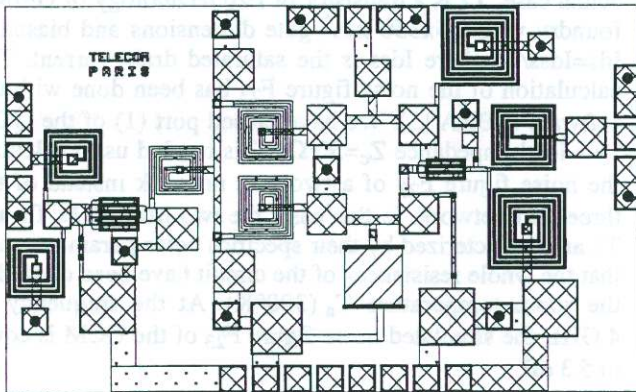


Figure 3: Layout of the quasi-circulator module.

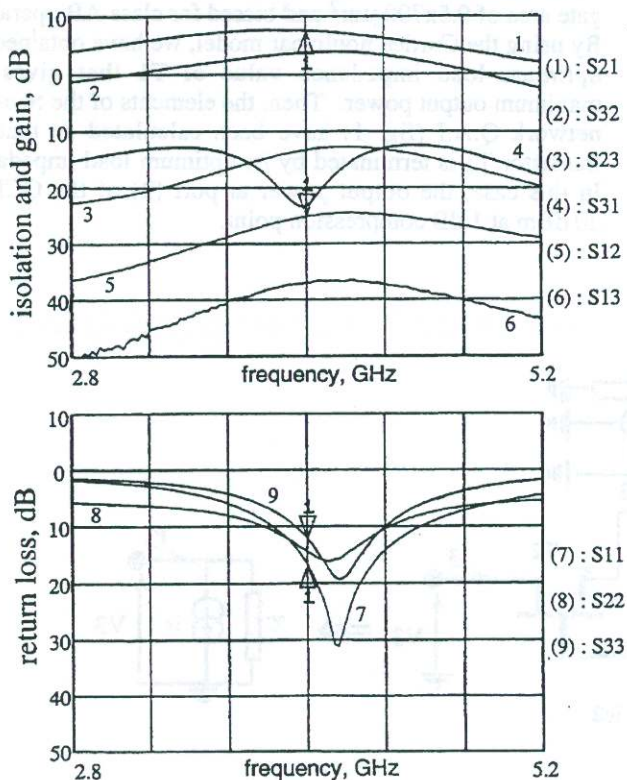


Figure 4: Measured frequency characteristics of the quasi-circulator.

of the transistor T2. Fig. 4 shows the measurement results of the QCM. For a frequency of 4 GHz, the circuit presents gain values of 7.6 dB and 4 dB between the transmitter-antenna ports and the antenna-receiver ports, respectively, and an isolation of 22 dB in the transmit-receive path. The minimum isolation of 13 dB in the receiver-antenna path is in most cases sufficient because the receiver is generally well matched. It can be noticed that the best return losses are obtained at 4.1 GHz instead of 4 GHz and are greater than 14 dB. This small frequency shift can be due to the coupling between elements, which was not taken into account during the simulation.

Fig. 5 shows the input-output power characteristics of the fabricated quasi-circulator. The circuit presents 18 dBm

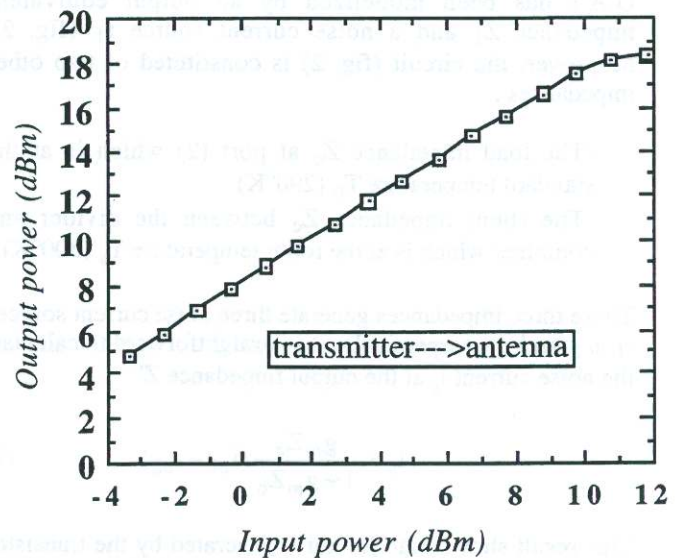


Figure 5: Handling power characteristics of the quasi-circulator.

output power at 1 dB compression point. The measured noise figure F_{23} between port (2) and port (3) is 5.5 dB.

Finally, it is important to note that this circuit can handle very high power between ports (1) and (2) by simply increasing the width of the transistor T1. The noise figure F_{23} will always have the same value because it is independent of the noise generated by T1.

Conclusion

This study has proved the design for a quasi-circulator module allowing to transport simultaneously a medium power signal from transmitter to antenna and a low power signal from antenna to receiver. This circuit can be used to transmit very high power by increasing the width of the divider transistor T1. The characteristics of the QCM concerning the power capability and the noise figure can be improved using HEMT technology with well appropriate transistors T1 and T2.

References

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Abstract

The second harmonic generation efficiency of a non-uniform non-linear transmission line (NLTL) has been theoretically investigated by using a static equivalent circuit model. The NLTL is a cascade of two identical NLTLs and two identical NLTLs. The efficiency of the NLTL for frequency doubling is improved by using an input impedance matching network.

Introduction

Non-linear transmission lines (NLTLs) are commonly used for pulse compression via the generation of short waves and solitons and for harmonic generation purposes [1]. A typical NLTL is composed of series inductors connected by shunt-connected non-linear capacitors. Usually, the first case are tested by means of equivalent circuit models, and the second case by means of Schottky diodes. Recently, non-uniform NLTLs have been proposed for high pulse compression ratio [2]. The elementary cell of the structure is depicted in Fig. 1.

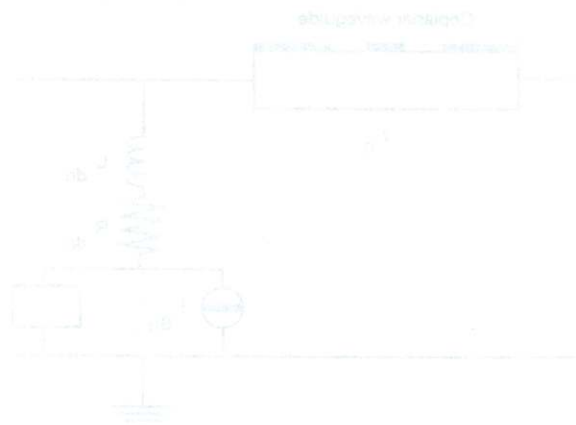


Fig. 1 Elementary cell of a non-uniform NLTL. The NLTL is a cascade of two identical NLTLs and two identical NLTLs. The efficiency of the NLTL for frequency doubling is improved by using an input impedance matching network.

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$$I_{in} = I_{out} \times \left(\frac{1}{1 + \frac{R_L}{R_0}} \right) \quad (1)$$

$$I_{in} = I_{out} \times \left(\frac{1}{1 + \frac{R_L}{R_0}} \right) \quad (2)$$

where I_{in} is the input current, I_{out} is the output current, R_L is the load resistance, and R_0 is the characteristic impedance of the NLTL.

In this paper, the second harmonic generation efficiency of a non-uniform NLTL structure has been theoretically investigated for harmonic generation by using a static equivalent circuit model. The NLTL is a cascade of two identical NLTLs and two identical NLTLs.